IN THE SPECIFICATION

Please replace the following paragraphs and add the new paragraphs in the Brief Description of the Drawings, starting at page 4, as follows:

For paragraph [0020], please amend as follows:

FIG. 10 depicts a top view layout of a first embodiment the HHISCR protection device of FIG. 9; ~~and~~

For paragraph [0021], please amend as follows:

FIG. 11 depicts a top view layout of a second embodiment the HHISCR protection device of FIG. 9[[.]];

Please insert the following new paragraphs [0021.1] through [0021.4] between paragraphs [0021] and [0022] as follows:

FIG. 12 depicts a schematic diagram of a hybrid HHISCR protection device having a plurality of HHISCR ESD protection device slices;

FIGS. 13-16 depict a top view and respective cross-section layouts of various embodiments of the hybrid HHISCR protection device of FIG. 12;

FIG. 17 depicts a schematic diagram of a second embodiment of a hybrid HHISCR protection device having an SCR and GGNMOS trigger device formed in parallel slices; and

FIG. 18 depicts a top view of the hybrid HHISCR protection device of FIG. 17.

Please replace the following paragraphs and add the new paragraphs in the Detailed Description of the Invention as follows:

Please replace paragraph [0029] with the following amended paragraph:

[0029] ~~Alternately~~ Alternatively, where the second gate 134 of the SCR 106 is used, a second trigger device 108_2 is coupled between the second gate G2 134 and ground 112, while a second low resistance shunt resistor 110_2 is coupled from the voltage supply line 114 to the second gate G2 134. In a third embodiment and as shown below in FIG. 3, both first and second trigger devices 108_1 and 108_2 and the low resistance shunt resistors 110_1 and 110_2 are respectively coupled to the first and second gates 136 and 134 as described above.

Please replace paragraph [0030] with the following amended paragraph:

[0030] In one embodiment, the trigger devices 108 may be MOS devices, e.g., a grounded gate NMOS (GGNMOS) device or a source-connected gate PMOS (SGPMOS) device. ~~Alternately~~ Alternatively, the trigger devices may be a Zener diode in a reverse conduction direction, a small diode chain in a forward conduction direction, or other devices typically used in the art.

Please replace paragraph [0032] with the following amended paragraph:

[0032] In one embodiment, the shunt resistors 110 are external on-chip resistors fabricated from, for example, silicided poly-silicon, and are selected with a resistance value (e.g., 0.1-10 ohms), which is much lower than the intrinsic substrate resistance R_{sub} 130. The first and second resistors 110_1 and 110_2 serve as shunts for respectively directing currents to ground 112 or from the supply 114. As such, the first and second shunt resistors 110_1 and 110_2 are respectively in parallel with the base-emitter diodes of the NPN transistor 116 and PNP transistor ~~114~~ 118 of the SCR. The shunt resistors 110 provide a path for undesirable leakage currents between the trigger devices 108

and ground 112 or the supply 114, respectively, which otherwise might unintentionally trigger the SCR 106. Furthermore, the low resistance resistors 110 will control the so-called trigger and holding currents of the SCR 106, as is described in detail below.

Please replace paragraph [0042] with the following amended paragraph:

[0042] FIG. 2 depicts a graph of current and voltage characteristics 200 for the HHISCR ESD protection device 102 of the present invention. The graph comprises an ordinate 202 representing current characteristics of the ESD protection device 102, and an abscissa 204 representing voltage characteristics of the ESD protection device 102. The voltage characteristic is divided into three regions defined by particular voltages. In particular, a first region 206 is defined from zero volts to the actual supply voltage of the IC 100. The actual voltage may be any supply voltage required for IC operation. A second region 208 is defined above the supply voltage and below an over-voltage condition. A third region 210 for an over-voltage condition has a range of voltage transients that are considered harmful to the gate oxides ~~oxide~~ of the IC 100. The latch-up current I_{lu} is normally specified at 100 milliamps or 300 milliamps, which are typical industry standards.

Please replace paragraph [0044] with the following amended paragraph:

[0044] Referring to curve 212, which represents normal operation of the IC 100 (general HHISCR of FIG. 1, as well as powered AC-HHISCRs), the general HHISCR protection device 102 is designed to have a trigger voltage V_{trig} greater than the supply voltage VDD, and less than V_{max}. Thus, the trigger voltage V_{trig} occurs in the second region 208 of the IV characteristics 200 for the HHSCR protection device 102. Additionally, the holding voltage V_h or $V_{h\text{-}op}$ has a potential less than the voltage of the supply line to be protected (e.g., VDD). Further, the HHISCR protection device 102 has a trigger current I_{trig} that is greater than the latch-up current I_{lu}. Moreover, the holding current I_{OP} or [[$I_{l\text{-}op}$]] $I_{H\text{-}op}$ is greater than latch-up current I_{lu} (but not necessarily in case of hysterisis effects). Providing the holding currents above the specified latch-

up current during normal IC operation helps provide latch-up immunity and interference with the functionality of the IC 100.

Please replace paragraph [0045] with the following amended paragraph:

[0045] Referring to curve 214, which represents a non-powered condition for the actively controlled HHISCR of the IC 100, the HHISCR protection device 102 also has a holding voltage ~~$V_{h\text{-}op}$~~ $V_{h\text{-}ESD}$ that is less than the voltage supply line to be protected (e.g., VDD). More importantly, in this non-powered state, the trigger current I_{trig} is less than the latch-up current I_{lu}, in contrast to the trigger current I_{trig} being greater than the latch-up current I_{lu}, during a powered condition. As such, the SCR 106 will quickly trigger during an ESD event when the IC 100 is in a non-powered state. As will be discussed regarding the actively controlled HHISCR embodiments depicted in FIGS. 3-8, the inventive SCR protection device 102 has a holding current $I_{H\text{-}ESD}$, under non-powered IC ESD conditions, below the specified latch-up current I_{lu} of the HHISCR protection device 102.

Please replace paragraph [0050] with the following amended paragraph:

[0050] During normal operation with the IC 100 powered on, the latch-up control circuits 312 are coupled to the variable resistors 310, which couples the gates G1 136 and G2 134 of the SCR 106 to the respective supply lines. ~~via the low resistance variable resistors 310.~~ That is, gate G1 136 is coupled to ground 112 via low resistance variable resistor 310_1, and gate G2 134 is coupled to the protected supply line 104 via a low resistance variable resistor 310_2. The variable resistors 310 ~~has~~ have a low resistance value between 0.1 and 10 ohms. As such, the triggering and holding currents are above the latch-up current of the SCR 106, as shown in FIG. 2.

Please replace paragraph [0053] with the following amended paragraph:

[0053] FIG. 4 depicts a schematic block diagram of an actively controlled

HHISCR protection device 402 having multiple SCR fingers 106. FIG. 4 is the same as the embodiment of FIG. 3, except that the trigger devices 108, variable shunt resistors 110, and latch-up control circuits may be used to provide triggering and holding currents above the latch-up currents for multiple SCR fingers 106_1 through 106_n (where n is an integer greater than one). For a typical layout implementation of a multifinger SCR, including placement of trigger gates, the reader is directed to commonly assigned U.S. Patent Application Serial No. 09/974,011, filed October 10, 2001 by Sarnoff Corporation of Princeton, New Jersey, which is incorporated herein by reference in its entirety.

Please replace paragraph [0058] with the following amended paragraph:

[0058] Similarly, the P-well 504 comprises a plurality of N+ doped regions 510_1 through 510_n and a plurality of P+ doped regions 514_1 through 514_m, where a P+ doped region 514 is interspersed between adjacent N+ doped regions 510. For example, P+ region 514_1 is positioned between N+ regions 510_1 and 510_2. Further, each high doped N+ and P+ doped region ~~518~~ 510 and 514 are separated by a portion of the P-well 504, such as P-well portions 518_1 and 518_p, as shown in FIG. 5. The P+ and N+ doped regions 508 and 510, respectively with the proximate areas of the N-well and P-well regions 502 and 504, together form SCR slices 106_q, where q is an integer greater than one. For example, P+ and N+ doped regions 508_1 and 510_1, respectively with the proximate areas of the N-well and P-well regions 502 and 504, together form a first SCR slice 106_1, and so forth.

Please replace paragraph [0060] with the following amended paragraph:

[0060] The length of each P+ region 508 and N+ region 510 is a determining factor for achieving trigger currents above the specified latch-up current of the SCR 106. In particular, a length L_A of each P+ region 508 forming the anode 122 is equal to the length L_C of each N+ region 510 forming the cathode 140. The actual lengths L_A and L_C of the P+ anode regions 508 and the N+ cathode regions 510 may vary according to the trigger and holding currents that are desired by the HHISCR protection device 102. In

one embodiment, the lengths L_A and L_C of the P+ and N+ regions 508 and 510 are in a range of 0.16 to 10 micrometers. Furthermore, the lengths L_{G1} and L_{G2} of the respective P+ an N+ regions ~~518~~ 514 and 512, which form the first and second trigger taps have lengths in the range of 0.2 to 2 micrometers.

Please replace paragraph [0062] with the following amended paragraph:

[0062] It is also noted that reducing the lengths L_A of the P+ regions 508 allows the adjacent trigger taps of the second gate G2 134 to be in closer proximity to each other. Likewise, reducing the lengths L_C of the N+ regions 510 allows the adjacent trigger taps of the first gate G1 136 to be in closer proximity to each other. In one embodiment, the distance 516 between the P+ regions 508 and N+ regions 512 in the N-well 502 are between 0.12 and 1.2 micrometers. Likewise, the distance 518 between the N+ regions 510 and P+ regions ~~518~~ 514 in the P-well 504 are between 0.12 and 1.2 micrometers. As such, the number and lengths L_A and L_C of the P+ and N+ doped regions 508 and 510, in relation to the interspersed trigger gate taps G1 136 and G2 134, affect the triggering and holding currents of the HHISCR device 102.

Please replace paragraph [0065] with the following amended paragraph:

[0065] FIG. 6 illustratively shows the trigger devices 108 and the latch-up control circuits 312 for both SCR gates G1 and G2 136 and 134. The HHISCR ESD protection device 602 is used to provide a high triggering and holding current under normal IC operation (above the specified latch-up current). Conversely, the HHISCR ESD protection device 602 is used to provide a low triggering and holding current to facilitate easy triggering during an ESD event, when the IC 100 is in an off state, as shown in FIG. 2. ~~In particular, the~~ The trigger and holding currents are below the specified latch-up current because the latch-up criterion is not applicable for an un-powered IC 100 during ESD.

Please replace paragraph [0069] with the following amended paragraph:

[0069] FIG. 6 illustratively shows a Zener diode Z_{lu} coupled in the reverse conduction direction between the protected supply line 104 and the second node 634. ~~Alternately~~ Alternatively, a capacitor C_{lu} or GGNMOS device may also be utilized as a trigger device 634. It is noted that the control circuit 606 is shared by both latch-up control circuits 312_1 and 312_2, and is required in any of the embodiments using either or both the first trigger gate 136 and/or the second trigger gate 134.

Please replace paragraph [0072] with the following amended paragraph:

[0072] Pulling the gate of the NMOS transistor N_{lu} 608 to ground 112, turns the NMOS transistor N_{lu} 608 off. Once the NMOS transistor N_{lu} 608 is off, the resistor R_{ld} 604 (i.e., P-substrate resistance 128, and optionally the parallel shunt resistor 110 of FIG. 1) is coupled between the first trigger gate 136 and ground 112. As such, the SCR 106 will trigger when the voltage across the trigger device T1 ~~108_2~~ 108_1 produces current flow through the resistor R_{ld} 604 and the voltage across the resistor R_{ld} 604 rises to approximately 0.7 volts, which forward biases the base-emitter diode D_n of the NPN transistor 116. The current regeneration process of the SCR 106 begins and causes the SCR 106 to shunt the ESD current to ground 112. It is important to note that the high resistance of the effective resistor R_{ld} 604 causes the triggering current I_{trig} and holding current I_{hold} during to be lower than the latch-up current I_{lu}, as shown by curve 214 of FIG. 2.

Please replace paragraph [0074] with the following amended paragraph:

[0074] Alternately, during a non-powered state of the IC 100, the gate of the PMOS transistor P_{lu} 614 is high, which turns the PMOS transistor P_{lu} 614 off. As such, the second gate G2 134 is floating, which lowers the triggering current I_{trig} and holding current I_{hold} of the SCR 106 below the latch-up current I_{lu}, as shown by curve 214 of FIG. 2. Triggering during an ESD event by the second trigger device 108_2 pulls the trigger gate G2 134 lower, causing a voltage drop across the emitter-base diode D_p of

the PNP transistor ~~181~~ 118 and starting the regenerative conduction in the SCR 106.

Please replace paragraph [0075] with the following amended paragraph:

[0075] It is readily seen that the latch-up control circuits 312 utilize the exemplary NMOS and PMOS transistors 608 and 614, in conjunction with the intrinsic resistance R_{sub} 130, optional shunt resistors 110, and N-well resistor 132, to provide the effective resistance of the variable shunt resistors 310, as shown in FIGS. 3, 4, and 6. It is noted that the RC delay with respect to the first pulldown resistor R1 620 and the capacitor C_{LU} must be at least in the order of magnitude of the rise time of the ESD pulse, since the latch-up control circuit 312 needs to be inactive during SCR triggering (i.e. consequently node 636 is pulled high during the rising edge of the ESD pulse, and the latch-up control devices 312 are in off mode). After the SCR "latches" into high current operation, the gates of the SCR 106 have minor impact on SCR operation, such that renewed activation of the latch-up control devices 312 has no influence on the function of the ESD protection. It is further noted that ~~alternate~~ alternative embodiments of the common control circuit 606 may also be utilized, as illustratively discussed with regard to FIG. 7 below.

Please replace paragraph [0081] with the following amended paragraph:

[0081] Once the PMOS transistor P_{dd} 708 is turned on, the first node 632 is pulled high to the protected supply line 104. The PMOS transistor P_c 610 is then turned off and the NMOS transistor N_c 612 is turned on, thereby pulling the gate of the NMOS transistor N_{lu} 608 to ground 112 and turning off the NMOS transistor N_{lu} 608. Once the NMOS transistor N_{lu} 608 is off, then only the resistor R_{ld} 604 is coupled between the first trigger gate 136 and ground 112. Therefore, a much larger portion of the current from the trigger device 108_1 ~~108_2~~ is now fed into the trigger gate G1 136 of the SCR for further turn-on. That is, the SCR 106 will trigger when the voltage across the resistor R_{ld} 604 rises to approximately 0.7 volts, which forward biases the base-emitter diode D_n of

the NPN transistor 116. The forward biasing of the base-emitter diode D_n begins the current regeneration of the SCR 106 to shunt the ESD current.

Please replace paragraph [0094] with the following amended paragraph:

[0094] When the IC 100 is not powered, the parasitic capacitances 316 between the supply lines 804 are not charged. In particular, the gate and the source of the PMOS transistor P_{lu} 614 are pulled capacitively to ground 112, thereby turning the PMOS transistor P_{lu} 614 off. Once the PMOS transistor P_{lu} 614 is off, the second trigger gate G2 134 can now be considered floating. As such, the second trigger gate G2 134 is pulled low after triggering of the second trigger element ~~108_1~~ 108_2. The PMOS transistor P_{LU} off decreases the triggering and holding current of the SCR 106 during an ESD event to the desired low values. In fact, the triggering I_{trig} and holding currents I_{hold} are below the latch-up current I_{lu}, as shown by curve 214 of FIG. 2.

Please replace paragraph [00104] with the following amended paragraph:

[00104] The SGPMOS and GGNMOS transistors 906 and 908 are apportioned and integrated with each slice 106_q. For example, a portion of the P+ doped region 508_1 in the N-well 502 forms the emitter of the PNP transistor 118, as well as the source of the SGPMOS transistor ~~908~~ 906, which are coupled to the anode 122. The drain of the SGPMOS transistor ~~908~~ 906 is formed in a second P+ doped region 1012 in the N-well 502 and is connected to the cathode 140 via metallic path 1004. The gate 1016 of the SGPMOS transistor ~~908~~ 906 is formed between and perpendicular to the P+ doped region 508 second P+ doped region 1012, and is coupled to the anode 122 via path 1006.

Please replace paragraph [00105] with the following amended paragraph:

[00105] Similarly, a portion of the N+ doped region 510_1 in the P-well 504 forms the emitter of the NPN transistor 116, as well as the source of the GGNMOS transistor ~~906~~

908 which is coupled to the cathode 140. The drain of the GGNMOS transistor ~~906~~ 908 is formed in a second N+ doped region 1020 in the P-well 504, and is connected to the anode 122 via metallic path 1008. The gate 1024 of the GGNMOS transistor ~~906~~ 908 is formed between and perpendicular to the N+ doped region 510 and second N+ region ~~1024~~ 1020, and is coupled to the cathode 140 via path 1010.